In the Specification

Please amend Paragraph 0054 as follows:

Thus, for example, in FIGS. 7a - 7b, nominal-voltage decoupling capacitor 214 and high-voltage decoupling capacitor 215 are depicted having a minimum of complexity. These depicted embodiments are at a stage of a process flow technique modified by an integration method of the present invention for forming any number, combination, and/or type of inventive decoupling capacitors, CMOS FinFET's, and/or other devices on the same substrate in order to provide effective decoupling capacitance in an area-efficient manner. Particularly, wafer 202 is depicted with an overlying buried insulator 204. On top of buried insulator 204 are nominal-voltage decoupling capacitor 214 and high-voltage decoupling capacitor 215. Nominal-voltage decoupling capacitor 214 comprises narrow semiconductor layer 206 portion (the narrow Fin) with overlying thick hard mask film 208 narrow line. Insulator layers 210 are formed on opposing vertical sidewalls of the narrow Fin. As seen in FIG. 7b, the top surface of the insulator layers 210 is adjacent to the hard mask film 208 (i.e., height of the top surface of the insulator layers 210 is greater than the height of the lower surface of the hard mask film 208 and less the height of the upper surface of the hard mask film 208, wherein each of said heights are relative to the top surface of the buried insulator 204). Conductor layer 212 portion is structured adjacent insulator layer 210 portions and hard mask film 208 narrow line portion, thereby encapsulating the narrow Fin. High-voltage decoupling capacitor 215 comprises broad semiconductor layer 206 portion (the broad Fin) with overlying thick hard mask film 208 narrow line. Insulator layers 210 are formed on opposing vertical sidewalls of the broad Fin. Conductor layer 212 portion is structured adjacent hard mask film 208 broad line portion so that conductor layer 212 portion is

within a thickness of the broad Fin. It is advantageous for the conductor layer 212 portion to partially overlay (or be within the thickness) of the broad Fin. If conductor layer 212 portion extended beyond the thickness of the broad Fin, thereby becoming additionally adjacent to a sidewall of the broad Fin, then a region of thin insulator on the sidewall would be exposed to high electric fields when using this decoupling capacitor at higher voltages. This would result in significantly higher leakage currents through the capacitor and in decreased reliability. For the capacitor 215, the thickness of the Fin 206 is T_{F1} and the thickness of the conductor layer 212 is T_{C1}. For the capacitor 214, the thickness of the Fin 206 is T_{F2} and the thickness of the conductor layer 212 is T_{C2}. As seen in FIGS. 7a-7b for the capacitor 215, the thickness of the conductor layer 212 is within the thickness of the Fin 206, which means in FIGS. 7a-7b and in the claims that $T_{C1}<T_{F1}$ such that the sidewalls 11 and 12 of the conductor layer 212 are each disposed between the sidewalls 21 and 22 of the Fin 206 as shown. Also as seen in FIGS. 7a-7b for the capacitor 214, the thickness of the Fin 206 is within the thickness of the conductor layer 212, which means in FIGS. 7a-7b and in the claims that $T_{F2}<T_{C2}$ such that the sidewalls 41 and 42 of the Fin 206 are each disposed between the sidewalls 31 and 32 of the conductor layer 212 as shown. FIGS. 7a-7b also show that $T_{F1}>T_{F2}$.